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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,747	LAUFFER ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-15 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9-15 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/16/06 has been entered. Applicants have amended claims 1-6 and 13-15. Claims 7-8 and 16-21 are cancelled. Claims 22-25 are newly added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-6, 9, 11-15, and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. (US 20040150969).

Regarding claim 1, as shown in figures 1 and 7-8, Chan discloses a circuitized substrate comprising:

(a) First and second dielectric layers 23 (two layers of dielectric material, top and bottom, see paragraph 25), each of the first (top) and second (bottom) dielectric layer 23 having first and second opposing sides (inner and outer side);

(b) a substantially solid conductive ground plane 21/106 (power or ground plane, paragraphs 25 and 38 and see examiner remarks below) located between the first opposing side of the first dielectric layer and the first opposing side of the second dielectric layer;

(c) a first conductive signal line 25/105 (paragraph 25 and 38 and selectively the rightmost signal line 105 of the left pair on the top surface) located on the second opposing side of the first dielectric layer and a second conductive line 27/105 (paragraph 25 and 38 and selectively the rightmost signal line 105 of the left pair on the bottom surface) located on the second opposing side of the second dielectric laver;

(d) first (the left 101) and second (the right 101) conductive ground lines 101 (shielding, paragraph 38) located on the second opposing side of the first dielectric layer on opposite sides of the first conductive signal line and electrically coupled to the substantially solid conductive ground plane 106 located on the first opposing side of the dielectric layer; and

(e) as shown in figure 1, a first conductive thru-hole 29 (see examiner remarks below) extending through the substantially solid conductive ground plane and electrically coupling the first conductive signal line to the second conductive signal line, the first (left) and second (right) conductive ground lines 101 and the substantially conductive ground plane 106 providing shielding for the at least one conductive signal line during the passage of electrical current through the signal line (shielding, see paragraph 38).

Examiner remarks:

(a) The conductive planes 21 or 106 of figures 1 and 8: Chan preferred the plane to serve as a power lane, but the plane does not have to serve as a power plane but a ground plane depending on the operational requirements of the final board (see paragraph 29 and 34).

(b) The conductive thru-hole 29 connecting the top and bottom signal lines shown in figure 1: Chan does not have to show the through hole in the embodiment shown in figure 8; because conductive thru-hole is known in connecting signal lines in different layers and figure 8 is mainly centering about the shielding, therefore Chan does not have to show the thru-hole again in figure 8. Thus, inherently a first conductive thru-hole 29 extending through the substantially solid conductive ground plane 106 and electrically coupling the first conductive signal line 105 (top) to the second conductive signal line 105 (bottom).

Regarding claim 3, Chan discloses the substantially solid conductive ground plane which is comprised of copper (paragraph 26).

Regarding claim 4, Chan discloses each of the first and second conductive signal lines which is comprised of copper (paragraph 26).

Regarding claim 5, Chan discloses the first and second conductive ground lines that are each comprised of copper (paragraph 26).

Regarding claim 6, as clearly shown in figure 8, Chan discloses second and third conductive thru-holes 103 (paragraph 38), the second and third conductive thru-holes electrically couple the first and second conductive ground lines 101 to the conductive ground plane 106.

Regarding claim 9, as shown in figures 2-6, Chan discloses additional dielectric and conductive layers as part thereof (multilayer printed circuit board).

Regarding claim 11, as clearly shown in figure 3, Chan discloses the circuitized substrate (top section of the multilayer circuit board 30) which is a chip carrier (semiconductor chip 77 on the surface, paragraph 33).

Regarding claim 12, Chan discloses the circuitized substrate which is a printed circuit board (see abstract).

Regarding claim 13, as shown in figure 8, Chan discloses every limitation as shown in claim 1 above and further including a third conductive signal line 105 (selectively the leftmost signal line 105 of the right pair on the top surface) positioned on the second opposing side of the first dielectric layer adjacent the first conductive signal line (also 105), the first and second conductive ground lines 101 and the substantially solid conductive ground plane 106 also providing shielding for the third conductive signal line 105 during the passage of electrical current through said third conductive signal line.

Regarding claim 14, as shown in figure 8, Chan further discloses a conductive ground line 101 (the center line 101) positioned on the second opposing side of the first dielectric layer substantially between the first and third conductive signal lines 105, the conductive ground line 101 also providing shielding for the first and third conductive signal lines during the passage of electrical current through the first and third conductive signal lines 105.

Regarding claim 15, as shown in figure 2, Chan discloses every limitation as shown in claim 1 above and further including third and fourth dielectric layers 81 (paragraph 34) positioned on the first and second dielectric layers 23 respectively, and

second and third substantially solid conductive ground planes 83 (paragraph 34) positioned on the third and fourth dielectric layers 81, respectively, the second and third substantially solid conductive ground planes 83 also providing shielding for the at least one conductive signal line during the passage of electrical current through the signal line.

Regarding claims 22-25, Chan discloses every limitation as shown in the above claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 20040150969).

Regarding claim 2, Chan discloses every limitation as shown in claim 1 above but fails to disclose the first and second dielectric layer are each selected from fiberglass-reinforced polymer resin.

Dielectric layer material such as fiberglass-reinforced polymer resin is old and well known in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select fiberglass-reinforced polymer resin as a preferred dielectric material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 10, as shown in figures 2-6, Chan disclose every limitation as shown in claim 9 above, but fails to disclose first and second pluralities of external conductive pads located on opposite sides of the circuitized substrate for electrically coupling the circuitized substrate to external electrical components.

Surface mounting pads are old and known in the art for mounting external components (semiconductor chip for example) on a surface of a circuit board.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include first and second pluralities of external conductive pads located on opposite sides of the circuitized substrate for electrically coupling the circuitized substrate to external electrical components (semiconductor chips) for the operation of the circuit board.

Response to Arguments

7. Applicant's arguments with respect to claims 1-6 and 9-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
8/29/06